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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
COURTENAY III, ST JOHN	
ART UNIT	**PAPER NUMBER**
2194	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,833	WILLIAMS ET AL.	
	Examiner	Art Unit	
	St. John Courtenay III	2194	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,9-15,19 and 20* is/are rejected.

7)☒ Claim(s) *6-8 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

ST. JOHN COURTENAY III
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Response to Amendment

New grounds of rejection are set forth responsive to Applicant's amendments and arguments. The Examiner does not agree that adding the limitation of a "message pipeline FIFO" to the independent claims renders the claims patentable, as message pipeline FIFOs are notoriously well known in the multiprocessor art, as evidenced by the **Yamada** reference relied upon as teaching this feature (previously cited in the office action mailed May 19, 2004), and also by new references cited in this office action.

However, responsive to Applicant's arguments, the Examiner has reconsidered the rejections of dependent claims 6, 7, 8, 16, 17, and 18, as set forth in the last office action.

In light of Applicant's arguments of record, dependent claims 6, 7, 8, 16, 17, and 18 appear to be allowable over the prior art of record if rewritten to include all of the limitations of the base claim and any intervening claims, subject to the results of a final search. These claims stand objected to as being dependent upon a rejected base claim.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 4, 5, 9-15, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Orr et al.** (U.S. Patent 4,862,350) in view of **Yamada** et al. (U.S. Patent 5,617,537).

As per independent claim 1:
Orr teaches an apparatus comprising:

- a system bus [e.g., see "ADDRESS" and "DATA" buses shown in fig. 2, and associated discussion, col. 6, lines 41-49]; Note: the instant specification broadly discloses a "bus 110" (page 5, line 6) without specifying a particular type of bus; when the "broadest reasonable interpretation consistent with the specification" examination standard is properly applied, any type of prior art bus (e.g., a data bus, an address bus, or a control bus) reasonably reads upon the broad scope of the claimed "system bus"];

- a shared memory [see shared message buffer 20, fig. 2, col. 6, line 28],
  - (i) coupled to the system bus [e.g., see "ADDRESS" and "DATA" buses shown in fig. 2, and associated discussion, col. 6, lines 41-49]; and,
  - (ii) configured to store data [col. 4, lines 25-30]; and

- a multiprocessor logic circuit comprising:
  - (i) a plurality of processors [see primary processor 10 and master processor 32 as shown in figs. 1 & 2; see associated discussion col. 4, line 64], and
  - (ii) a message circuit [e.g., see "CONTROL INTERFACE 44" as shown in fig. 2 and associated discussion, beginning col. 6, line 25], wherein,

    - (a) the message circuit is a directly connected to the system bus and configured to pass messages between the plurality of processors [see direct

connection to the system ADDRESS bus, as shown in fig. 2; see associated discussion col. 6, line 39], and,

- (b) each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus [see direct connection between processors 10 & 32 via the common ADDRESS bus and common DATA bus as shown in fig. 2 (e.g., functioning as "system" buses); see also associated discussion beginning col. 6, line 38].

Orr discloses the invention substantially as claimed, as discussed above.

However, **Orr** does not *explicitly* teach the following additional limitations:

Yamada teaches the use of a message circuit comprising a message pipe-line FIFO, as claimed [e.g., see "FIFO communication area" and associated discussion, beginning col. 7, line 50; col. 8, lines 45-65; see, in particular, the "FIFO communication area" discussion col. 11, lines 56-67, cont'd col. 12, lines 1-5, see associated Fig. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by **Orr** by implementing the improvements detailed above because it would provide **Orr's** system with the enhanced capability of asynchronous send and receive processing [e.g., see Yamada col. 8, lines 45-63].

As per independent claim 12:
This claim is rejected for the same reasons detailed above in the rejection of independent claim 1, and also for the following additional reasons:

Orr teaches an apparatus comprising:

- means for storing data with a shared memory [see shared message buffer 20, fig. 2, col. 6, line 28; see also col. 4, lines 25-30];

- means for processing data with a plurality of processors, wherein each of the plurality of processors is directly-connected to a system bus [see direct connection between processors 10 & 32 via the common ADDRESS bus and common DATA bus as shown in fig. 2 (e.g., functioning as "system" buses)];

- means for passing messages between the processors, wherein the message passing means is directly connected to the system bus [e.g., see "CONTROL INTERFACE 44" as shown in fig. 2 and associated discussion, beginning col. 6, line 25]; and

- means for coupling each of the processors to the shared memory, wherein the shared memory and the message by each of the plurality of passing means are accessible processors through a the system bus [see the coupling of processors 32 & 10 to shared memory 20, via the common DATA and ADDRESS buses, as shown in fig. 2; see also associated discussion beginning col. 6, line 38].

As per independent claim 13:
This claim is rejected for the same reasons detailed above in the rejection of the preceding independent claims, and also for the following additional reasons:

Orr teaches a method for multiprocessor communication with a shared memory, comprising the steps of:

(A) storing data with the shared memory [see shared message buffer 20, fig. 2, col. 6, line 28; see also col. 4, lines 25-30];

(B) processing data with a plurality of processors [see direct connection between processors 10 & 32 via the common ADDRESS bus and common DATA bus as shown in fig. 2 (e.g., functioning as "system" buses)]; and

(C) passing messages between the processors with a message circuit, wherein (i) each of the plurality of processors and the message circuit are directly connected to a system bus [e.g., see "CONTROL INTERFACE 44" as shown in fig. 2 and associated discussion, beginning col. 6, line 25] and (ii) each of the plurality of processors is configured to access the shared memory and the message circuit through the system bus [see direct connection between processors 10 & 32 via the common ADDRESS bus and common DATA bus as shown in fig. 2 (e.g., functioning as "system" buses) ; see also associated discussion beginning col. 6, line 38].

As per dependent claim 2:
Orr teaches the message circuit comprises a dedicated messaging circuit [e.g., see "FIG. 2 shows a more detailed block diagram of **control interface 44**. The interface allows primary

processor 10 and the master processor 32 to share message buffer 20." and associated discussion, beginning col. 6, line 25].

As per dependent claim 4:
Orr teaches the message circuit is further configured to provide bi-directional orderly command passing [e.g., see " Since the address and data buses of both processors are coupled to the shared message buffer, each processor has the ability to address the shared buffer and extract or place information at desired addresses within the buffer. ", and associated discussion, beginning col. 6, line 45; see also "Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through **control interface 44**."].

As per dependent claim 5:
Orr teaches the message circuit (i.e., "control interface 44") is further configured to generate one or more control signals configured to control an operation of the plurality of processors [e.g., see " Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through **control interface 44**." and associated discussion, beginning col. 7, line 6].

As per dependent claim 9:
Orr teaches the multiprocessor logic circuit further comprises an address decoder configured to decode a system address and control the message circuit [see "combinatorial logic means A1 and A2" and associated discussion col. 7, lines 11-15].

As per dependent claim 10:
Orr teaches the apparatus provides a multiprocessor communication and shared memory architecture [e.g., see Figs. 1 & 2, and associated discussion beginning col. 2, line 54].

As per dependent claim 11:
Orr teaches the multiprocessor logic block further comprises an address decoder configured to generate one or more first control signals configured to control the message circuit [e.g., see "FIG. 2 shows a more detailed block diagram of **control interface 44**. The interface allows primary processor 10 and the master processor 32 to share message buffer 20." and associated discussion, beginning col. 6, line 25]; and
the message circuit is configured to generate one or more second control signals configured to control the processors [e.g., see " Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through **control interface 44**." and associated discussion, beginning col. 7, line 6; see also: "the function of the control interface 44 is to generate the necessary handshaking signals which are required to pass control of the shared buffer from the master processor 32 to the primary processor 10 and vice versa." Col. 5, lines 8-13].

As per dependent claim 14:
Orr teaches step (C) further comprises providing bi-directional orderly command passing [e.g., see " Since the address and data buses of both processors are coupled to the shared message buffer, each processor has the ability to address the shared buffer and extract or place information at desired addresses within the buffer. ", and associated discussion, beginning col. 6, line 45; see also "Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through **control interface 44**."].

As per dependent claim 15:
Orr teaches step (C) further comprises generating one or more control signals, the control signals configured to control an operation of the processors [e.g., see " Still referring to FIG. 2, the handshaking and control for the accessing of the shared memory is done through **control interface 44**." and associated

discussion, beginning col. 7, line 6; see also: "FIG. 2 shows a more detailed block diagram of **control interface 44**. The interface allows primary processor 10 and the master processor 32 to share message buffer 20."; see also: "the function of the control interface 44 is to generate the necessary handshaking signals which are required to pass control of the shared buffer from the master processor 32 to the primary processor 10 and vice versa." Col. 5, lines 8-13].

As per dependent claim 19:
Orr teaches decoding a system address [see address decode logic means A1 and A2, and associated discussion col. 8, line 16].

As per dependent claim 20:
Orr teaches controlling the messages in response to the decoded system address [see address decode logic means A1 and A2, and associated discussion col. 8, line 16].

Claims 1, 2, 4, 5, 9-15, 19, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Fletcher et al.** (U.S. Patent 4,862,350) in view of **Yamada** et al. (U.S. Patent 5,617,537).

As per independent claim 1:
Fletcher teaches an apparatus comprising:

- a system bus [e.g., see ADDRESS BUS = "A" and DATA BUS = "D" and CONTROL BUS = "C" as shown in fig. 1, and associated discussion, col. 5, lines 50-60]; Note: the instant specification broadly discloses a "bus 110" (page 5, line 6) without specifying a particular type of bus; when the "broadest reasonable interpretation consistent with the specification" examination standard is properly applied, any type of prior art bus (e.g., a data bus, an address bus, or a control bus) reasonably reads upon the broad scope of the claimed "system bus"];

- a shared memory [see shared cache (S) 10 and SHARED MAIN STORAGE 36 as shown in fig. 1, col. 6, line 37, line 65, respectively],
  - (i) coupled to the system bus [e.g., see ADDRESS or A bus shown in fig. 1, and discussed col. 5, lines 50-60]; and,
  - (ii) configured to store data [inherent]; and

- a multiprocessor logic circuit comprising:
  - (i) a plurality of processors [see "PROCESSOR A" 4 and "PROCESSOR B" 6, as shown in fig. 1; see associated discussion col. 5, beginning line 26], and
  - (ii) a message circuit [e.g., see "CACHE CONTROL & DIRECTORY 22" and/or "STORAGE CONTROL (SCU) 38" as shown in fig. 1 and associated discussion, beginning col. 5, lines 40 and 49, respectively], wherein,

- (a) the message circuit is a directly connected to the system bus and configured to pass messages between the plurality of processors [see direct connection to the system ADDRESS and CONTROL buses (A & C) as shown in fig. 1; see associated discussion cols. 5 and 6; the SCU 38 is also shown directly connected to the data bus "D" 47], and,

- (b) each of the plurality of processors is directly connected to the system bus and configured to access the shared memory and the message circuit through the system bus [see direct connection between processors A & B (4 & 6) via the ADDRESS bus and DATA buses as shown in fig. 1 (e.g., functioning as "system" buses); see also associated discussion cols. 5 & 6].

However, **Fletcher** does not *explicitly* teach the following additional limitations:

Yamada teaches the use of a message circuit comprising *a* message pipe-line FIFO, as claimed [e.g., see "FIFO communication area" and associated discussion, beginning col. 7, line 50; col. 8, lines 45-65; see, in particular, the "FIFO communication area" discussion col. 11, lines 56-67, cont'd col. 12, lines 1-5, see associated Fig. 4].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to improve upon the system taught by **Fletcher** by implementing the improvements detailed above because it would provide **Fletcher's** system with the enhanced capability of asynchronous send and receive processing [e.g., see Yamada col. 8, lines 45-63].

As per independent claim 12:
This claim is rejected for the same reasons detailed above in the rejection of independent claim 1 under **Fletcher**, as modified by **Yamada**, and also for the following additional reasons:

Fletcher teaches an apparatus comprising:

- means for storing data with a shared memory [see shared cache (S) 10 and SHARED MAIN STORAGE 36 as shown in fig. 1, col. 6, line 37, line 65, respectively];

- means for processing data with a plurality of processors [see "PROCESSOR A" 4 and "PROCESSOR B" 6, as shown in fig. 1; see associated discussion col. 5, beginning line 26], wherein each of the plurality of processors is directly-connected to a system bus [e.g., see ADDRESS BUS = "A" and DATA BUS = "D" and CONTROL BUS = "C" as shown in fig. 1, and associated discussion, col. 5, lines 50-60]; Note: the instant specification broadly discloses a "bus 110" (page 5, line 6) without specifying a particular type of bus; when the "broadest reasonable interpretation consistent with the specification" examination standard is properly applied, any type of prior art bus (e.g., a data bus, an address bus, or a control bus) reasonably reads upon the broad scope of the claimed "system bus"];

- means for passing messages between the processors, wherein the message passing means is directly connected to the system bus [e.g., see "CACHE CONTROL & DIRECTORY 22" and/or "STORAGE CONTROL (SCU) 38" as shown in fig. 1 and associated discussion, beginning col. 5, lines 40 and 49, respectively]; and

- means for coupling each of the processors (see PROCESSORS A & B, 4 & 6, respectfully as shown in fig. 1)

to the shared memory, wherein the shared memory and the message by each of the plurality of passing means are accessible processors through a system bus [see direct connection between processors A & B (4 & 6) via the DATA bus to the SHARED CACHE (S) 10, and the coupled connected to the SHARED MAIN STORAGE 36, as shown in fig. 1 (e.g., functioning as "system" buses); see also associated discussion cols. 5 & 6].

As per independent claim 13:
This claim is rejected for the same reasons detailed above in the rejection of the preceding independent claims under **Fletcher**, as modified by **Yamada**, and also for the following additional reasons:

Fletcher teaches a method for multiprocessor communication with a shared memory, comprising the steps of:

(A) storing data with the shared memory [see shared cache (S) 10 and SHARED MAIN STORAGE 36 as shown in fig. 1, col. 6, line 37, line 65, respectively];

(B) processing data with a plurality of processors [see "PROCESSOR A" 4 and "PROCESSOR B" 6, as shown in fig. 1; see associated discussion col. 5, beginning line 26]; and

(C) passing messages between the processors with a message circuit [e.g., see "CACHE CONTROL & DIRECTORY 22" and/or "STORAGE CONTROL (SCU) 38" as shown in fig. 1 and associated discussion, beginning col. 5, lines 40 and 49, respectively], wherein (i) each of the plurality of processors and the message circuit are directly connected to a system bus [e.g., see ADDRESS BUS = "A" and DATA BUS = "D" and CONTROL BUS = "C" as shown

in fig. 1, and associated discussion, col. 5, lines 50-60]; Note: the instant specification broadly discloses a "bus 110" (page 5, line 6) without specifying a particular type of bus; when the "broadest reasonable interpretation consistent with the specification" examination standard is properly applied, any type of prior art bus (e.g., a data bus, an address bus, or a control bus) reasonably reads upon the broad scope of the claimed "system bus"] and (ii) each of the plurality of processors is configured to access the shared memory and the message circuit through the system bus [see direct connection between processors A & B (4 & 6) via the ADDRESS bus and DATA buses as shown in fig. 1 (e.g., functioning as "system" buses); see also associated discussion cols. 5 & 6].

As per dependent claim 2:
Fletcher teaches the message circuit comprises a dedicated messaging circuit [e.g., see "CACHE CONTROL & DIRECTORY 22" and/or "STORAGE CONTROL (SCU) 38" as shown in fig. 1 and associated discussion, beginning col. 5, lines 40 and 49, respectively].

As per dependent claim 4:
Fletcher teaches the message circuit is further configured to provide bi-directional orderly command passing [e.g., see SCU discussion, e.g., col. 5, lines 64-66].

As per dependent claim 5:
Fletcher teaches the message circuit (i.e., "CACHE CONTROL & DIRECTORY 22" and/or "STORAGE CONTROL (SCU) 38) is further configured to generate one or more control signals configured to control an operation of the plurality of processors [col. 5, lines 64-66, i.e., "SCU 38 **controls** all communication between main storage 36 and the respective processors and caches"].

As per dependent claim 9:
Fletcher teaches the multiprocessor logic circuit further comprises an address decoder configured to decode a system address and control the message circuit [e.g., see "ADDRESS LOGIC" networks 192 & 202, and associated discussion, beginning col. 10, line 33].

As per dependent claim 10:
Fletcher teaches the apparatus provides a multiprocessor communication and shared memory architecture [see PROCESSORS A & B, 4 & 6, respectfully as shown in fig. 1; see shared cache (S) 10 and SHARED MAIN STORAGE 36 as shown in fig. 1, col. 6, line 37, line 65, respectively].

As per dependent claim 11:
Fletcher teaches the multiprocessor logic block further comprises an address decoder configured to generate one or more first control signals configured to control the message circuit [e.g., see "ADDRESS LOGIC" networks 192 & 202, and associated discussion, beginning col. 10, line 33].

As per dependent claim 14:
Fletcher teaches step (C) further comprises providing bi-directional orderly command passing [e.g., see SCU discussion, e.g., col. 5, lines 64-66].

As per dependent claim 15:
Fletcher teaches step (C) further comprises generating one or more control signals, the control signals configured to control an operation of the processors [col. 5, lines 64-66, i.e., "SCU 38 **controls** all communication between main storage 36 and the respective processors and caches"].

As per dependent claim 19:
Fletcher teaches decoding a system address [e.g., see "ADDRESS LOGIC" networks 192 & 202, and associated discussion, beginning col. 10, line 33].

As per dependent claim 20:
Fletcher teaches controlling the messages in response to the decoded system address [e.g., see "ADDRESS LOGIC" networks 192 & 202, and associated discussion, beginning col. 10, line 33].

Prior Art not relied upon:
Please refer to the references listed on the attached PTO-892 which are not relied upon in the claim rejections detailed above.

How to Contact the Examiner:

Any inquiry concerning this communication or earlier communications from the examiner should be directed to St. John Courtenay III, whose telephone number is 571-272-3761. A voice mail service is also available at this number. The Examiner can normally be reached on Monday - Friday, 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, An Meng-AI who can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

All responses sent by U.S. Mail should be mailed to:

Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

New USPTO Patents Central FAX Number Starting July 15, 2005

On July 15, 2005, the Central Facsimile (FAX) Number will change from 703-872-9306 to 571-273-8300. Faxes sent to the old number will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and 571-273-8300 will be the only facsimile number recognized for "centralized delivery."

- Any inquiry of a general nature or relating to the status of this application should be directed to the **TC 2100 Group receptionist: (571) 272-2100.**

ST. JOHN COURTENAY III
PRIMARY EXAMINER